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09/755,825	01/05/2001	Iain Robertson	TI-28925	5403

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EXAMINER	
KADING, JOSHUA A	

ART UNIT	PAPER NUMBER
2661	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/755,825	Applicant(s) ROBERTSON ET AL.	
	Examiner Joshua Kading	Art Unit 2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-13 and 15* is/are rejected.

7)☒ Claim(s) *8 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 8, 10, and 14 are objected to because of the following informalities:

Claim 8, line 8 states "indicates also contains". This does not make sense and should be changed to one of the following --also indicates-- and --also contains--.

Claim 10, lines 33 and lines 35-36 state, "and second transmit ring" and "and second receive ring" respectively. This should be changed to --and the second transmit ring-- and --and the second receive ring--.

Claim 14, line 5 states "the valid line". For clarity, this should be changed to --the read valid line--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finney et al. (U.S. Patent 5,487,092) in view of Alston (U.S. Patent 6,055,285).

Regarding claim 1, Finney discloses "an interface circuit for communicating received data from a receive clock domain into a transmit clock domain, comprising:

a buffer, comprising a plurality of entries, having an input coupled to receive data from the receive clock domain and having an output for presenting data into the transmit clock domain (figure 1, element 38 represents a buffer with a plurality of entries and elements 14 and 20 show the two clock domains); and

a plurality of valid logic circuits, each associated with a corresponding one of the plurality of entries of the buffer (figure 1, element 36 is the valid logic for each entry; figure 3 shows a more detailed view of the valid logic circuits for each entry), each valid logic circuit comprising:

a read valid latch for controlling the state of a valid line in the transmit clock domain, the read valid latch having a reset input coupled to receive a read request signal (figure 3, element 48 it should be noted that although figure 3 does not show the latch having a reset input, it is well known in the art that latches of all kinds have reset inputs on them)..."

set logic for setting the read valid latch responsive to the write request signal (col. 5, lines 56-61 and figure 3, where the signal from element 46 into valid latch 48 indicates the data is read to be written into the appropriate entry in buffer 38,)."

However, Finney lacks what Alston discloses, that is "...a write valid latch for controlling the state of a valid line in the receive clock domain, the write valid latch having a set input coupled to receive a write request signal (figure 2, element 140 acts as the latch)...reset logic for resetting the write valid latch responsive to the read request signal (col. 7, lines 44-63 whereby inhibiting the ACK signal is the functional equivalent of resetting the latch so that it will not write and the wrong time, specifically while a read operation is in progress or when the pointers are updating)..."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the write valid latch and the reset logic for the purpose of not having data mistakenly written into a buffer entry before it has been read out from the buffer. The motivation is the preservation of unread data so it may be properly transmitted before it is overwritten.

Regarding claim 2, Finney and Alston disclose the interface of claim 1. However, Finney lacks what Alston further discloses, that is "write pointer logic for maintaining a write pointer indicating one of the entries of the buffer into which a next received data word is to be written from the receive clock domain (figure 2, element 122 and col.7, lines 17-23); and read pointer logic for maintaining a read pointer indicating one of the entries of the buffer from which a next data word is to be read into the transmit clock

domain (figure 2, element 132 and col. 7, lines 32-41)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the pointers with the interface of claim 1 for the same reasons and motivation as in claim 1.

Regarding claim 5, Finney discloses "a method of transferring data words from a receive clock domain into a transmit clock domain, comprising the steps of:

applying a data word to an input of a buffer having a plurality of entries (col. 5, lines 11-13);

responsive to a write valid bit associated with a first one of the plurality of entries indicating that the first one of the plurality of entries does not contain valid data...storing the applied data word into the first one of the plurality of entries (col. 5, lines 41-63);

setting the write valid bit associated with the first one of the plurality of entries (col. 5, lines 57-63 where the V1 flag bit is the functional equivalent of the write valid bit because it signifies when the information in the corresponding register is ready to be written); and

setting a read valid bit associated with the first one of the plurality of entries (col. 5, lines 56-63 where the R1 flag bit is the functional equivalent of the read valid bit because it signifies when the data is ready to be read into registers 38); and

responsive to a read valid bit associated with a second one of the plurality of entries indicating that a second one of the plurality of entries contains valid data (figure 1, where all of the registers 28 have read valid bits)...

reading the contents of the second one of the plurality of entries into the transmit clock domain (col. 5, lines 56-63 again when both valid bits are set the data is read from the first clock domain into the second clock domain);

clearing the read valid bit associated with the second one of the plurality of entries; and clearing a write valid bit associated with the second one of the plurality of entries (figure 2, elements 48 and Read Flag R1 clearly show the resetting of both flag bits)."

However, Finney lacks what Alston discloses, that is "the first one of the plurality of entries indicated by a current value of a write pointer (figure 2, element 122 and col.7, lines 17-23)... the second one of the plurality of entries indicated by a current value of a read pointer (figure 2, element 132 and col. 7, lines 32-41)..."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the write pointer and the read pointer for the purpose of not having data mistakenly written into a buffer entry before it has been read out from the buffer by way of using the values of the pointers to determine if the data has been read or not. The motivation is the preservation of unread data so it may be properly transmitted before it is overwritten.

Regarding claim 6, Finney and Alston disclose the method of claim 5. However, Finney lacks what Alston further discloses, that is "after the storing step, incrementing the write pointer (col.7, lines 17-23)." It would have been obvious to one with ordinary

skill in the art at the time of invention to include the incrementing of the pointer with the method of claim 5 for the same reasons and motivation as in claim 5.

Regarding claim 7, Finney and Alston disclose the method of claim 6. However, Finney lacks what Alston further discloses, that is "after the reading step, incrementing the read pointer (col.7, lines 32-41)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the incrementing of the pointer with the method of claim 6 for the same reasons and motivation as in claim 6.

Regarding claim 9, Finney and Alston disclose the method of claim 7. However, Alston lacks what Finney further discloses, that is "responsive to the read valid bit associated with a second one of the plurality of entries indicating that the second one of the plurality of entries does not contain valid data, issuing an idle symbol (col. 7, lines 13-18 where the RN bits are the read valid bits causing the pad word or idle symbol to be inserted into the data stream)."

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finney et al. and Alston as applied to claim 1 above, and further in view of Cassiday et al. (U.S. Patent 5,799,175).

Regarding claim 3, Finney and Alston disclose the interface of claim 1. However, Finney and Alston lack what Cassiday discloses, that is "a first edge detector circuit, for

detecting a transition of the read request signal in the transmit clock domain (figure 3, element 72 where edge detector 72 is part of a sync circuit 43)..."

However, Finney and Cassiday also lack what Alston further discloses, that is "...a first synchronizer circuit, having an input coupled to the first edge detector circuit, for generating, at an output coupled to a reset input of the write valid latch, a reset signal synchronized into the receive clock domain (figure 2, element 212 where the sync circuit 212 contains edge detector 72 of Cassiday and further supplies data to appropriately enable a reset signal (ACK signal in Alston) of the write valid latch as read in col. 7, lines 44-63)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the edge detector and synchronizer circuit with the interface of claim 1 for the purpose of not having data mistakenly written into a buffer entry before it has been read out from the buffer. The motivation is the preservation of unread data so it may be properly transmitted before it is overwritten.

Regarding claim 4, Finney, Alston, and Cassiday disclose the interface of claim 3. Finney, Alston, and Cassiday explicitly lack "a second edge detector circuit, for detecting a transition of the write request signal in the receive clock domain..." Although Finney, Alston, and Cassiday specifically lack "a second edge detector circuit", Cassiday does disclose a "first edge detector circuit" as in claim 3. And Alston further discloses what Finney and Cassiday further lack, that is "a second synchronizer circuit...for generating, at an output coupled to a set input of the read valid latch, a set

signal synchronized into the transmit clock domain (figure 2, element 210)." Thus it can be implied that both sync circuits in Alston function similarly and as such, it would have been obvious to have both sync circuits contain the edge detector of Cassiday. It further would have been obvious to one with ordinary skill in the art at the time of invention to include the second edge detector with the sync circuit with the interface of claim 3 for the same reasons and motivation as in claim 3.

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowe et al. (U.S. Patent 6,233,221 B1) in view of Finney et al. in further view of Alston.

Regarding claim 10, Lowe discloses "a switch system for a communications network, comprising:

a plurality of switches, each having an interface for connecting to one or more network elements; a plurality of switch fabric devices, each comprising: a plurality of switch interfaces, each coupled to an associated one of the plurality of switches (figure 2, elements 205 and 209 where it is commonly known in the art that switch fabrics contain a plurality of switches to operate on a plurality of data inputs);

a first receive ring interface, operating in a receive clock domain (figure 1 shows how the network element of figure 2 is incorporated into a ring network, figure 2 shows element 204 acting as a first receive ring interface);

a first transmit ring interface, operating in a transmit clock domain (figure 2, element 202 is a first transmit ring interface and it is well known that communication networks operate in clock domains)...

a first ring path, having an input coupled to the first ring receive interface and having an output (figure 1, where the inside ring is the first ring path)...

a second receive ring interface (figure 1, where each network element has a receive ring interface as described in figure 2, therefore there is at least a second receive ring interface in the network);

a second ring path, having an input coupled to the second ring receive interface and having an output (figure 1, where the outside ring is the second ring path);

a second transmit ring interface (figure 1, where each network element has a transmit ring interface as described in figure 2, therefore there is at least a second transmit ring interface in the network);

wherein the first receive ring interface and the second transmit ring interface correspond to a first ring interface that is coupled to a ring interface of another one of the plurality of switch fabric devices, and wherein the first transmit ring interface and the second receive ring interface correspond to a second ring interface that is coupled to a ring interface of another one of the plurality of switch fabric devices, such that the plurality of switch fabric devices are interconnected into a ring (figure 1 shows that each network element is connected through each of their respective interfaces and as pictured are arranged into a ring structure)."

However, Lowe lacks what Finney discloses, that is "a transmit clock generator circuit, for generating a clock signal for controlling the operation of the first transmit ring interface; and

...a buffer, comprising a plurality of entries, having an input coupled to receive data from the receive clock domain and having an output for presenting data into the transmit clock domain (figure 1, element 38 represents a buffer with a plurality of entries and elements 14 and 20 show the two clock domains); and

a plurality of valid logic circuits, each associated with a corresponding one of the plurality of entries of the buffer (figure 1, element 36 is the valid logic for each entry; figure 3 shows a more detailed view of the valid logic circuits for each entry), each valid logic circuit comprising:

a read valid latch for controlling the state of a valid line in the transmit clock domain, the read valid latch having a reset input coupled to receive a read request signal (figure 3, element 48 it should be noted that although figure 3 does not show the latch having a reset input, it is well known in the art that latches of all kinds have reset inputs on them)..."

set logic for setting the read valid latch responsive to the write request signal (col. 5, lines 56-61 and figure 3, where the signal from element 46 into valid latch 48 indicates the data is read to be written into the appropriate entry in buffer 38,)."

Further still, Lowe and Finney lack what Alston discloses, that is "...a write valid latch for controlling the state of a valid line in the receive clock domain, the write valid latch having a set input coupled to receive a write request signal (figure 2, element 140

acts as the latch)...reset logic for resetting the write valid latch responsive to the read request signal (col. 7, lines 44-63 whereby inhibiting the ACK signal is the functional equivalent of resetting the latch so that it will not write and the wrong time, specifically while a read operation is in progress or when the pointers are updating)..."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the ring network, the buffer and valid logic with the write valid latch and the reset logic for the purpose of not having data mistakenly written into a buffer entry before it has been read out from the buffer. The motivation is the preservation of unread data so it may be properly transmitted before it is overwritten.

Regarding claim 11, Lowe, Finney, and Alston disclose the system of claim 10. However, Lowe and Alston lack what Finney further discloses, that is "a decoder, for decoding code groups received from the first receive ring interface and for presenting data words corresponding to the decoded code groups to the buffer (figure 1, element 26); and an encoder, for encoding data words read from the buffer and presenting code groups corresponding to the encoded data words to the first transmit ring interface (figure 1, element 26 and col. 7, lines 13-18 where the act of adding the padded word is encoding the data which must be done by an encoder). It would have been obvious to one with ordinary skill in the art at the time of invention to include the decoder and encoder with the system of claim 10 for the same reasons and motivation as in claim 10.

Regarding claim 12, Lowe, Finney, and Alston disclose the system of claim 11. However, Lowe and Alston lack what Finney further discloses, that is "a first multiplexer, having a plurality of inputs, and having an output coupled to the encoder (figure 1, element 40); a ring path register, having an input coupled to the output of the buffer and having an output coupled to one of the plurality of inputs of the first multiplexer (figure 1, element 24); wherein each of the plurality of switch interfaces each have an output coupled to respective inputs of the first multiplexer (figure 1, element 12 where the inputs to element 10 are from the switch interfaces are described in Lowe)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the multiplexer and register with the system of claim 11 for the same reasons and motivation as in claim 11.

Regarding claim 13, Lowe, Finney, and Alston disclose the system of claim 12. However, Lowe and Finney lack what Alston discloses, that is "write pointer logic for maintaining a write pointer indicating one of the entries of the buffer into which a next received data word is to be written from the receive clock domain (figure 2, element 122 and col.7, lines 17-23); and read pointer logic for maintaining a read pointer indicating one of the entries of the buffer from which a next data word is to be read into the transmit clock domain (figure 2, element 132 and col. 7, lines 32-41)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the pointers with the system of claim 12 for the same reasons and motivation as in claim 12.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lowe et al., Finney et al., and Alston as applied to claim 10 above, and further in view of Cassiday et al.

Regarding claim 15, Lowe, Finney, and Alston disclose the system of claim 10. However, Lowe, Finney, and Alston lack what Cassiday discloses, that is "a first edge detector circuit, for detecting a transition of the read request signal in the transmit clock domain (figure 3, element 72 where edge detector 72 is part of a sync circuit 43)..."

However, Lowe, Finney, and Cassiday also lack what Alston further discloses, that is "...a first synchronizer circuit, having an input coupled to the first edge detector circuit, for generating, at an output coupled to a reset input of the write valid latch, a reset signal synchronized into the receive clock domain (figure 2, element 212 where the sync circuit 212 contains edge detector 72 of Cassiday and further supplies data to appropriately enable a reset signal (ACK signal in Alston) of the write valid latch as read in col. 7, lines 44-63)."

Further, Lowe, Finney, Alston, and Cassiday all lack "a second edge detector circuit, for detecting a transition of the write request signal in the receive clock domain..." Although Lowe, Finney, Alston, and Cassiday specifically lack "a second edge detector circuit", Cassiday does disclose the "first edge detector circuit" as mentioned above. And Alston further discloses what Lowe, Finney, and Cassiday further lack, that is "a second synchronizer circuit...for generating, at an output coupled to a set input of the read valid latch, a set signal synchronized into the transmit clock domain (figure 2, element 210)." Thus it can be implied that both sync circuits in Alston

function similarly and as such, it would have been obvious to have both sync circuits contain the edge detector of Cassiday. It further would have been obvious to one with ordinary skill in the art at the time of invention to include the second edge detector with the sync circuit with the system of claim 10 for the same reasons and motivation as in claim 10.

Allowable Subject Matter

Claims 8 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Kading whose telephone number is (703) 305-0342. The examiner can normally be reached on M-F: 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Olms can be reached on (703) 305-4703. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joshua Kading
Examiner
Art Unit 2661

May 27, 2004

KENNETH VANDERPUYE
PRIMARY EXAMINER